**Amendments to the Claims:**

**Listing of Claims:**

Claim 1 (currently amended): A method for fabricating a semiconductor device comprising:

providing a substrate, at least one first gate structure and at least one second gate structure being included on a surface of the substrate, both the first gate structure and the second gate structure having sidewalls;

performing a first ion implantation process to form a shallow-junction doping region of a first conductive type in the substrate next to each of the sidewalls of the first gate structure;

forming offset spaces on each of the sidewalls of the first gate structure and the second gate structure after performing the first ion implantation process; and

performing a second ion implantation process to form a shallow-junction doping region of a second conductive type in the substrate next to the offset spacer on each of the sidewalls of the second gate structure after forming the offset spacers.

Claim 2 (original): The method of claim 1 wherein the substrate comprises a silicon substrate or a silicon-on-insulator substrate.

Claim 3 (original): The method of claim 1 wherein both the first gate structure and the second gate structure comprise a polysilicon gate and a gate dielectric layer interposed between the polysilicon gate and the substrate.

Claim 4 (original): The method of claim 1 wherein a dopant of the first implantation process comprises phosphorous or arsenic, and the first gate structure is a gate of an input/output (I/O) NMOS.

Claim 5 (original): The method of claim 1 wherein the method for forming the offset

spacer on each of the sidewalls of the first gate structure and the second gate structure further comprises the following steps:

forming a dielectric layer on the surface of the substrate to cover the first gate structure and the second gate structure; and

performing a dry etching process to vertically remove the dielectric layer down to the surface of the substrate.

Claim 6 (original): The method of claim 5 wherein the dielectric layer is a tetra-ethyl-ortho-silicate (TEOS) oxide layer formed by a low temperature chemical vapor deposition (LPCVD) process at a temperature ranging from 650°C to 680°C.

Claim 7 (original): The method of claim 6 wherein a thickness of the TEOS oxide layer ranges from 170 to 210 angstroms (Å).

Claim 8 (original): The method of claim 1 wherein a dopant of the second ion implantation process is boron, and the second gate structure is a gate of an input/output (I/O) PMOS.

Claim 9 (original): The method of claim 1 wherein at least one third gate structure is included on the surface of the substrate, an offset spacer is simultaneously formed on each sidewall of the third gate structure when forming the offset spacers on each of the sidewalls of the first gate structure and the second gate structure.

Claim 10 (original): The method of claim 9 further comprising the following steps after performing the second ion implantation process:

forming a spacer layer on the surface of the substrate to cover the first gate structure, the second gate structure, the third gate structure, and the offset spacers on each of the sidewalls of the first gate structure, the second gate structure, and the third gate structure;

and

performing an etching process to form a spacer at sides of the first gate structure, the second gate structure, and the third gate structure.

Claim 11 (original): The method of claim 9 further comprising at least one third ion implantation process after performing the second ion implantation process to form a lightly doped drain region in the substrate next to the offset spacer on each of the sidewalls of the third gate structure.

Claim 12 (original): The method of claim 9 further comprising at least one pocket ion implantation process after performing the second ion implantation process to form a pocket doping region in the substrate at either side of the first gate structure, the second gate structure, and the third gate structure.

Claim 13 (original): The method of claim 10 further comprising at least one fourth ion implantation process after performing the etching process to form a source/drain region in the substrate next to the spacer at either side of the first gate structure, the second gate structure, and the third gate structure.

Claim 14 (original): The method of claim 1 wherein the step for forming the offset spacers on each of the sidewalls of the first gate structure and the second gate structure is used for improving the hot carrier immunity ability of the semiconductor device.

Claims 15-28 (canceled)